Feedback Amplifiers

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Abstract

In this laboratory experiment, we explore all four types of negative feedback topologies, by investigating the frequency response and loading effects of each circuit. We also experiment with multi-stage amplifiers, and their effect on phase margin and overall stability. When instability is encountered, we impliment a dominant-pole compensation scheme with an RC filter. Using positive feedback, we create a circuit with controlled oscillations to produce a sinusoidal waveform.

1 Introduction

The development of negative feedback theory is very important when working with high-gain amplifiers. The standard operation-amplifier has an open-loop gain of over 100,000. To control this massive gain and provide stability, we employ the methods of negative feedback. Negative feedback is the process of sampling the ouput value (either voltage or current), and returning a fraction of this output to affect the input signal, in a negative way. Negative here does not refer to an undesirable type of feedback, but rather that the sampled signal is mixed into the input signal with an opposite sign, thereby reducing the strength of the input signal:

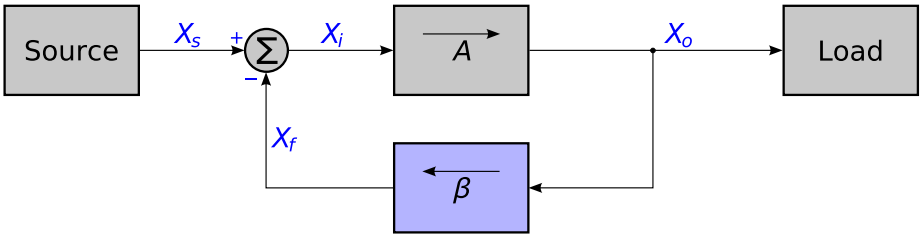

Figure 1: General Structure of Negative Feedback Amplifier

There are many advantages to negative feedback, including:

1. Reduction of noise and distortion.
2. Increase in amplifier bandwidth.
3. Modification of input and output impedances.
4. Desensitize the gain to factors such as temperature.

The main disadvantage to negative feedback is the large reduction in overall amplifier gain. We can therefore consider negative feedback to be a process by which we can trade-in gain to obtain better operating characteristics.

Each operational amplifier introduces what is know as a "pole", which is related to the complex frequency response of the amplifier. As the signal frequency increases, the phase shift between the input and output signal increases. Each pole can contribute a maximum of 90° to this phase shift. If the phase shift is ever equal to 180°, then the input and output signals will be exactly out of phase, with the input signal being low when the feedback signal is high. This is now positive feedback, and can lead to instability. When two op-amps are connected in a dual-stage amplifier, the phase shift will never reach 180°, as each op-amp can only contribute 90°. Unfortunately, when three op-amps are connected in a multi-stage amplifier, the maximum phase shift possible is 270°, well beyond the condition required for instability. When this occurs, we can employ a comensation strategy known as "dominant pole compensation", which is the method of introducting a new pole in the amplifier response at a low frequency, so that that gain has dropped to zero before the phase can get to 180°.

Normally, we use a frequency-independent feedback loop, that exhibits the same response over all frequencies. If the feedback loop was frequency-sensitive, we could use that to create a circuit that preferred a specific frequency. We employ this strategy, along with non-linear ampliutude control, to create a sine wave oscillator.

2 Experiments

2.1 Operational Amplifier Open Loop Gain

To get a baseline feeling for our operation amplifiers, we first need to measure the raw, open-loop gain of each of our available op-amp chips. We are using standard 741C op-amp chips, which have a nominal large signal voltage gain of 200,000[1]. Unfortunately, we cannot simply measure the DC voltage gain of an amplifier circuit, as this does not take into account the non-zero input offset voltage. We are using the schematic shown on page 3.

We want to create a very small voltage difference across the op-amp's terminals, so we use a 1000:1 voltage divider, using $10K\Omega$ and 10Ω resistors. It would be very difficult for the oscilloscope to measure such an insignificant voltage with any accuracy, so we simply measure at the point marked V_1. We know

[1] http://www.national.com/ds/LM/LM741.pdf

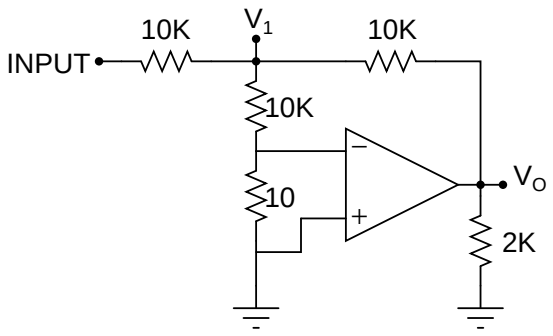

Figure 2: Circuit Schematic - Experiment 1

that the voltage measured there is actually 1000 times larger than the true differential input voltage. To mitigate the effects of the aforementioned non-zero input offset voltage, we need to take two measurements for each chip, and use the difference in their readings to find the open-loop voltage gain.

$$A_v = 1000 \left(\frac{V_{o1} - V_{o2}}{V_{i1} - V_{i2}} \right)$$

We have measured the data for each of our three op-amp chips:

Open-Loop Gain Data & Calculations

Chip #	V_s	V_i	V_o	A_v
1	5.02	-1.212	-8.610	980800
	0.0988	-1.207	-3.706	
2	5.03	-1.209	-8.640	618375
	0.0996	-1.201	-3.693	
3	5.01	-1.017	-8.02	446000
	0.1004	-1.006	-3.114	

As we can see, our op-amp chips had much higher open-loop voltage gains than predicted by the datasheet. The wide variance of measured gain reinforces the notion that inherent gain is not a good design parameter, and is not something to rely on. The use of negative feedback in our amplifier circuits enables us to ignore this variation, and de-sensitize our circuit's operation to gain variation from chip to chip.

2.2 Series/Shunt Topology

The first of the four negative feedback topologies we are investigating is the Series/Shunt topology. We are sampling the output voltage, and mixing a voltage back with the input signal. Using our circuit schematic on page 4, we can easily see that Series/Shunt is the correct topological assessment, as we are sampling

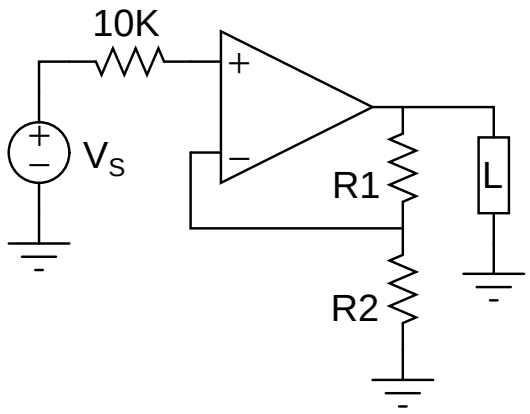

Figure 3: Circuit Schematic - Experiment 2

the output voltage using the R1/R2 voltage divider, and returning a fraction of the output voltage to offset the input voltage. We have designed our circuit to provide a voltage gain with no load of $15\frac{v}{v}$. Assumming an ideal opamp to solve this circuit, we know that there is no current through the $10K\Omega$ source resistance. This means that both op-amp terminals are equal to V_s. Using the voltage divider created by R1/R2, we know that:

$$V_s = V_o\left(\frac{R_2}{R_1+R_2}\right) \Rightarrow A_v = \frac{R_1+R_2}{R_2} = 1+\frac{R_1}{R_2}$$

For the specified no-load gain of 15, we can solve for R_1 and R_2:

$$15 = 1+\frac{R_1}{R_2} \Rightarrow R_1 = 14R_2 \Rightarrow \begin{cases} R_1 = 14K\Omega \\ R_2 = 1K\Omega \end{cases}$$

Since we do not have access to $14K\Omega$ resistors, we can construct an approximate equivalent by combining a $10K\Omega$ resitor and a $4.7K\Omega$ resistor.

There are a number of things we need to find for this circuit. Recording a frequency response is a very common operation when working with amplifiers. We do this by recording the input and output voltages for a wide range of frequencies, concentrating on the "corner frequency," when the amplifier's limitations start to affect the output waveform. We have measured the input voltage directly at the non-inverting terminal of the op-amp, and the output voltage at the output terminal of the op-amp. We used no load resistance for this basic frequency response measurement.

No-Load Frequency Response Data

Frequency (Hz)	V_{in}	V_o	A_v
10	0.319	4.800	15.05
100	0.306	4.560	14.90
1000	0.299	4.560	15.25
1800	0.300	4.560	15.20
3300	0.300	4.560	15.20
5600	0.298	4.560	15.30
10000	0.300	4.500	15.00
17000	0.297	4.370	14.71
33000	0.296	3.940	13.31
56000	0.294	3.260	11.09
58000	0.297	3.200	10.77
100000	0.297	2.200	7.41
330000	0.296	0.706	2.39
1000000	0.300	0.247	0.82

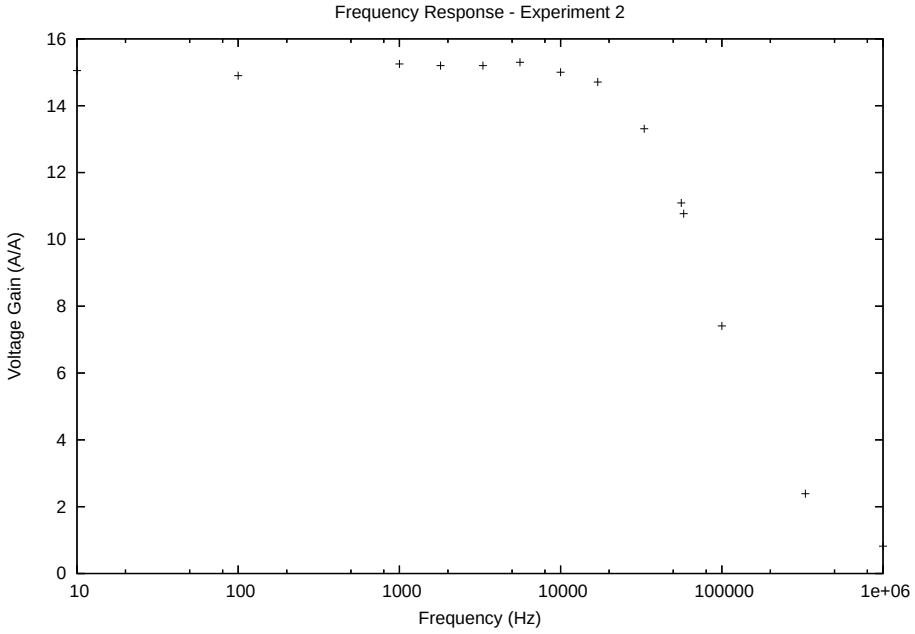

Figure 4: Frequency Response

As we can see, this is a fairly standard, one-pole amplifier frequency response. The maximum voltage gain is right around 15, which is the value we designed for. This is also the midband voltage gain. The corner frequency (dominant-pole) occurs when the gain is 10.82, which happens at a frequency of approximately

58 kHz. We can use this value, along with the amplifier's open-loop gain, to find the location of the dominant pole in the open-loop response, by relating the gain-bandwidth product for both open and closed loop configurations:

$$f_{-3dB,closed} \times A_{v,closed} = F_{-3dB,open} \times A_{v,open}$$

$$(58kHz)(15) = (F_{-3dB,open})(446000) \Rightarrow f = 1.96Hz$$

The dominant pole in the open loop response is located at approximately 1.95 Hz.

The data thus far has been collected with no load attached to the amplifier. When we connect a load, it draws current away from the feedback network. If the op-amp is able to provide enough current to maintain the output voltage at the same value, the circuit will continue to operate as normal. If the load resistance is too small, and draws too much current, the op-amp will become stressed, and the output voltage will drop as the op-amp reaches its maximum output current. We experimented with these loading effects using different values for the output resistance.

The other side of the coin, an amplifier's input resistance, can also be measured. Using Ohm's law, we can calculate the small-signal input resistance by measuring the input voltage and current. We can measure the small-signal input voltage by directly measuring the voltage of the non-inverting terminal of the op-amp. We can measure the small-signal input current by measu

Resistance (Ω)	A_v
10	2.32
47	8.79
100	14.69
1000	15.10
10000	15.98
∞ (open)	15.10

As we predicted, when the load resistance becomes too small, the op-amp is unable to provide enough current to maintain the proper output voltage. This is an important fact to remember, as we always try to design our amplifier stages with a very large input resistance, for this exact reason.

2.3 Shunt/Series Topology

Our second feedback topology is the Shunt/Series topology. This topology samples the output (load) current, and mixes current back in with the input current. We are using the circuit depicted on page 7. We can clearly see that the resistor labeled R2 is sampling the output current, while this sampled current is directly connected to the input current source. It is important to note that, due the the relative unavailability of current sources, we have approximated the current source with a voltage supply in series with a large ($1M\Omega$) resistor. We are designing for a mid-band, short-circuit current gain of 100. To solve this

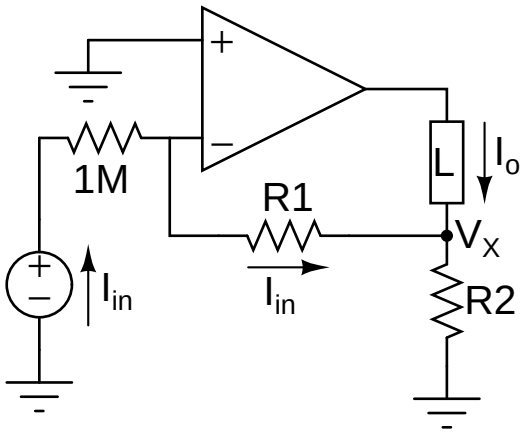

Figure 5: Circuit Schematic - Experiment 3

circuit, we first remind ourselves that the op-amp's terminals do not have any current flowing through them. This means that all of the input current is also going through the resistor labeled R1. We can then relate the input and output current, using a short-circuit load:

$$-I_{in} = I_o \left(\frac{R_2}{R_1 + R_2} \right) \Rightarrow A_i = \frac{-R_1 + -R_2}{R_2} = -1 - \frac{R_1}{R_2}$$

We are designing for a current gain of 100:

$$A_v = 100 = 1 + \frac{R_1}{R_2} \Rightarrow R_1 = 99R_2 \Rightarrow \begin{cases} R_1 = 100K\Omega \\ R_2 = 1K\Omega \end{cases}$$

For this circuit, we are interested in the effect of various sized loads on the current gain. The ideal case for no load is a short circuit, and we expect that as we increase the load resistance, the op-amp will be unable to provide a large enough voltage to keep the proper amount of current flowing through the load, as it will be limited both by the op-amp's internal voltage limits, and perhaps the rail voltages. To eliminate any potential error from frequency-dependent effects, we have performed the following measurements at a mid-band frequency of 1.0 kHz. We have measured the input voltage as the voltage at the positive terminal of the voltage supply. This is also the voltage across the $1M\Omega$ resistor, as the op-amp's inverting input is a virtual ground. This allows us to calculate the input current. To measure the output current, we have measured the voltage at V_x, which allows us to directly calculate the current through R_2. Since $R_1 >> R_2$, we can assume that the current through R_2 is equivalent to I_o. We can then directly calculate I_o from V_x. Once we have both I_{in} and I_o, we can then calculate A_i.

Loading Effects on Current Gain

Resistance (Ω)	V_{in}	V_x	$I_{in}(\mu A)$	$I_o(\mu A)$	A_i
0	0.968	0.097	0.965	96.500	99.690
100	0.968	0.096	0.968	96.400	99.580
1000	0.968	0.097	0.968	96.500	99.690
10000	0.968	0.096	0.968	96.400	99.580
100000	0.967	0.095	0.967	95.200	98.440
200000	0.966	0.094	0.966	93.500	96.790
400000	0.970	0.089	0.970	89.000	91.750
1000000	0.967	0.027	0.967	27.100	28.020
2000000	0.967	0.013	0.967	13.000	13.440

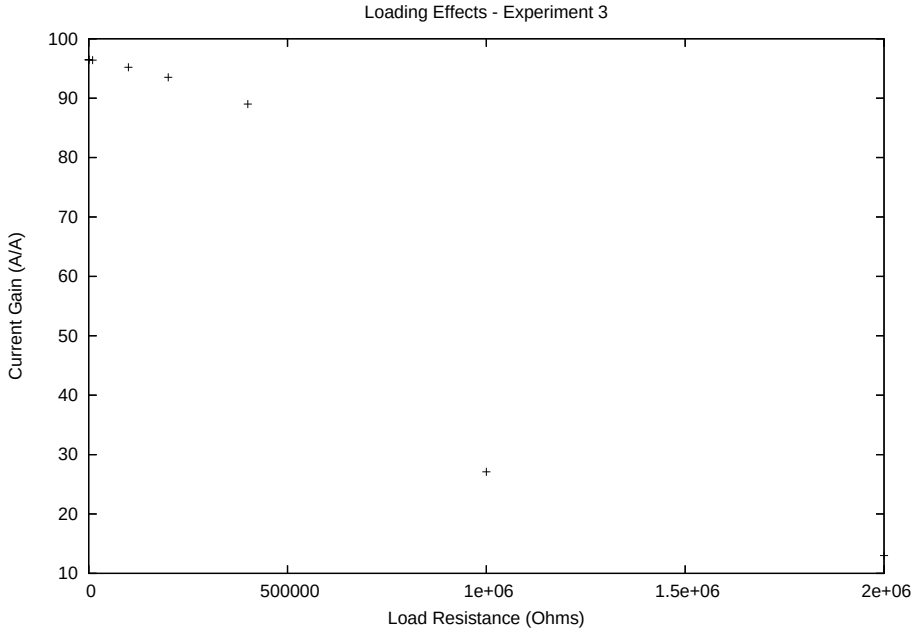

Figure 6: Loading Effects on Current Gain

As we predicted, the current gain did decrease as we increased the load resistance.

2.4 Series/Series Topology

The Series/Series feedback topology samples the output (load) current, and mixes it back in the form of a voltage. The circuit schematic for this experiment, located on page 9, shows how the resistor labeled R_f is sampling the load current, because the op-amp's terminals do not conduct any current. The

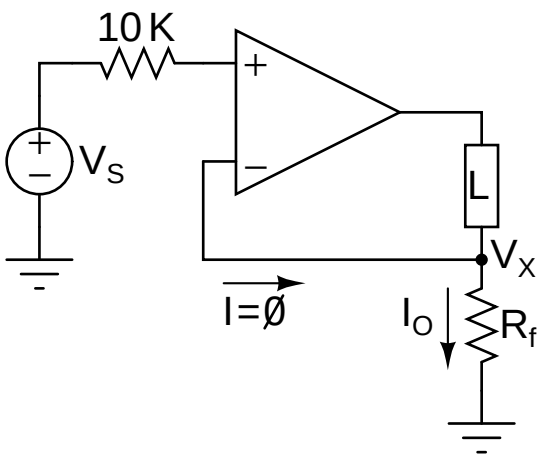

Figure 7: Circuit Schematic - Experiment 4

amount of load current directly affects the feedback voltage V_x. Note that the voltage at the input terminals is V_s, therefore $V_x = V_s$. We are trying to solve for the transconductance, $g_m = \frac{I_o}{V_{in}}$:

$$V_x = V_s = I_o R_f \Rightarrow \frac{I_o}{V_s} = R_f$$

We want to create a circuit with $g_m = 1\frac{ma}{v} = 1000$, and since $g_m = R_f$, we know to set $R_f = 1K\Omega$.

Again, we are interested in the loading effects of various load resistors on the circuit, specifically the effect on the transconductance. We have chosen to make measurements at a mid-band frequency of 1 kHz. We have measured the voltage at the voltage source, as well as at V_x. As discussed before, they should be nominally the same. Only when the load resistance is too high will V_s and V_x differ, as the op-amp stuggles to provide the necessary output voltage. Using V_x, we can directly calculate I_o, as $I_o = \frac{V_x}{1000}$.

Loading Effects on Transconductance (g_m)

Resistance (Ω)	V_{in}	V_x	$I_o(\mu A)$	$g_m(mA/V)$
0 (short)	1.000	1.020	1.020	1.020
1000	1.000	1.020	1.020	1.020
10000	1.000	1.020	1.020	1.020
50000	1.000	0.585	0.585	0.585
100000	1.000	0.330	0.330	0.330
1000000	1.000	0.340	0.034	0.034

Note that as the load resistance increases, the transconductance decreases.

2.5 Shunt/Shunt Topology

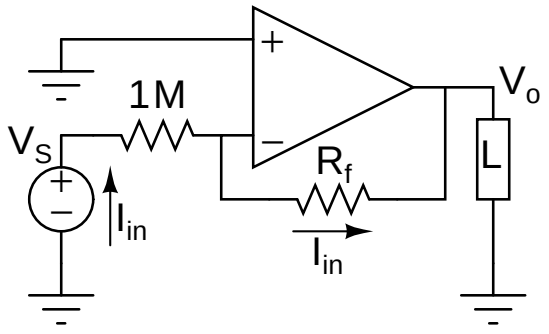

Figure 8: Circuit Schematic - Experiment 5

For the final feedback topology, we investigate the Shunt/Shunt topology. This topology has the characteristics of sampling the output voltage, and mixing current. Looking at the circuit schematic on page 10, we can see how the resistor labeled R_f is clearly sampling the output voltage compared to ground. The op-amp's input terminals are both grounded, because of the virtual-short between them, and the non-inverting input is grounded. Also, no current flows through the input terminals. This greatly simplifies the analysis, as we know that the input current is going straight through R_f. Depending on the value of V_o, additional current will be generated by the drop across R_f. We are trying to design for a transresistance of $r_m = 100K\Omega$. We know that $r_m = \frac{V_o}{I_{in}}$, so we can solve the circuit as such:

$$V_o = -I_{in}R_f \Rightarrow r_m = \frac{V_o}{I_{in}} = R_f$$

We are designing for $r_m = 100K\Omega$, so we set $R_f = 100K\Omega$.

We have measured the following values at a mid-band frequency of 1 kHz. We measured the input voltage directly at the voltage source, and measured the output voltage right at the output of the op-amp. Using the input voltage V_{in}, we can calculate the input current I_{in}. We are again interested in the effect of load resistances on the amplifier's performance. We predict that as the load is increased, and the op-amp is required to supply more and more current, eventually we will start to see loading effects manifested as decreased transresistance values.

Loading Effects on Transresistance (r_m)

Resistance (Ω)	V_{in}	$I_{in}(\mu A)$	V_o	$r_m(K\Omega)$
5	8.400	8.400	0.310	36.0
10	8.400	8.400	0.536	67.0
1000	0.968	0.968	0.103	106.4
10000	0.968	0.968	0.103	106.4
100000	0.968	0.968	0.103	106.4

2.6 Two-Stage Frequency Response

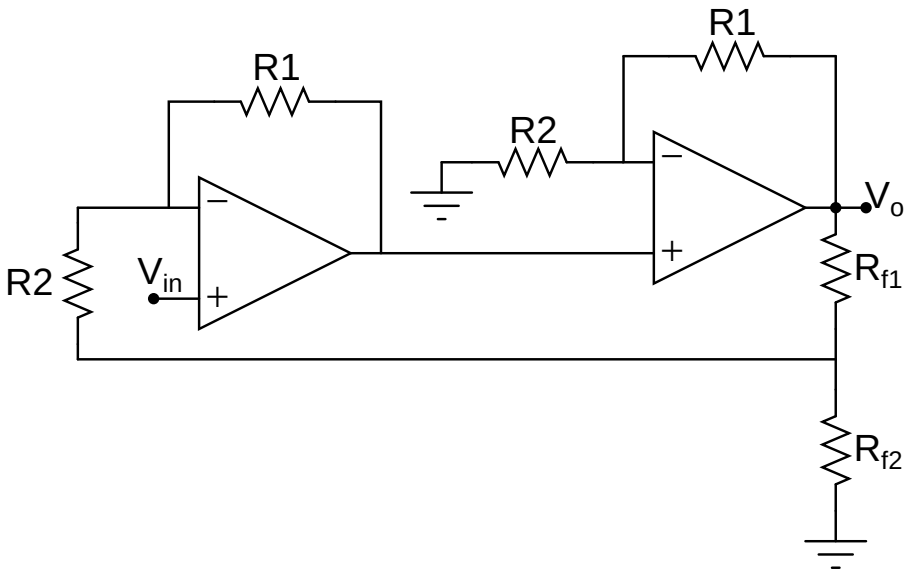

Figure 9: Circuit Schematic - Experiment 6

In this experiment, we connect two Series/Shunt amplifiers together, producing a combined open-loop gain of $15^2 = 225$. We can then use another feedback network to set the overall, closed-loop gain to 15. We recycle the same resistance values from Experiment 2, using $R_1 = 14K\Omega$ and $R_2 = 1K\Omega$. To solve for the new feedback resistors R_{f1} and R_{f2}, we can consider the two sub-amplifiers as one block amplifier, with an open-loop gain of 225, and solve from there. We find that, since this is the same arrangement as in Experiment 2,

$$A_v = 1 + \frac{R_{f1}}{R_{f2}} = 15 \Rightarrow R_{f1} = 14R_{f2} \Rightarrow \begin{cases} R_{f1} = 14K\Omega \\ R_{f2} = 1K\Omega \end{cases}$$

Using the specified resistor values, we then proceded to measure the frequency response. We measured the input voltage at the terminal of the first op-amp, and measured the output at the output terminal of the second op-amp.

Frequency Response Data

Frequency (Hz)	A_v
10	12.10
100	12.06
1000	12.06
10000	12.59
100000	14.34
200000	21.51
250000	24.40
300000	19.40
450000	7.04
600000	3.52
1000000	1.30

As we can see, this circuit has some resonance, indicated by the peak in the gain around 250 kHz. This peak has a gain value of approximately 24.4. We can find the Q-value of this circuit by finding the two corner frequencies on both sides of the resonance freqency. These two corner frequencies occur when the gain is $0.707 \times 24.4 = 17.25$. This occurs for frequencies of 155 kHz and 315 kHz. To calculate Q:

$$Q = \frac{f_\omega}{f_{c2} - f_{c1}} = \frac{250000}{315000 - 115000} = 1.25$$

We are also interested in the amplifier response for square wave input signals. We know that each op-amp has a limited slew rate, that is, there is a minimum time required for the op-amp to switch states. This is most evident when amplifying square waves at high frequencies. Immediately after switching states, the op-amp's output exhibits a "ringing" effect, where the output has a decaying exponential sinusoidal component, before settling to the proper value. This is directly observable using the oscilloscope, and we have included a sample trace on page 13.

We did not encounter any problems with the dc offset voltage being amplified by subsequent stages. Some students were having saturation problems caused by the second op-amp amplifying the dc offset voltage produced by the first op-amp.

2.7 Three-Stage Amplifier Stability

As noted in the introduction, when three amplifiers are combined in a multistage arrangement, the phase shift can be large enough to cause positive feedback, which causes massive instability in the amplifier's output. In this experiment, we combine three Series/Shunt amplifiers together, and observe the instability it produces. Using the circuit schematic depicted on page 13, we design for a variable voltage gain between 10 and 100. We can use a potentiometer in series with a standard resistor for R_{f1}, and another standard resistor for R_{f2}.

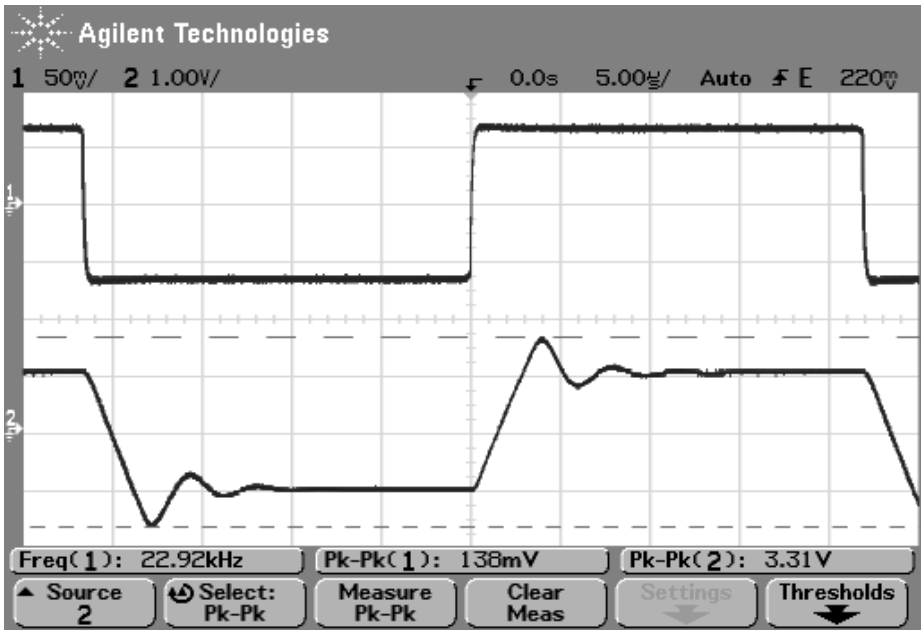

Figure 10: Square Wave Ringing Effect - Experiment 6

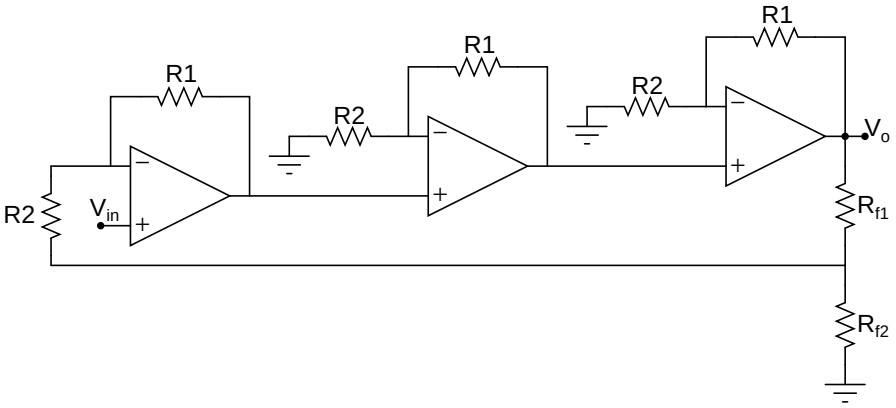

Figure 11: Circuit Schematic - Experiment 7

We can write two equations, one for when the gain is 10, and one for when the gain is 100:

$$10 = \frac{a}{b}, 100 = \frac{a + 10K\Omega}{b}$$

$$10b = 100b - 10K\Omega$$

$$10K\Omega = 90b \Rightarrow \begin{cases} a = 1110\Omega \\ b = 110\Omega \end{cases}$$

Using these values for a and b, we know that

$$\begin{cases} R_{f2} = b = 110\Omega \\ R_{f1} = a + (0 \rightarrow 10K\Omega) = 1110\Omega + (0 \rightarrow 10K\Omega) \end{cases}$$

Using these resistances, we can obtain a closed-loop gain between 11.09 and 102.

When we first connected this circuit, we immediately noticed that the output was not stable. When we turned the potentiometer to produce low gain, around 11, the instability increased, making the output waveform almost indecypherable. An oscilloscope trace is included on page 14.

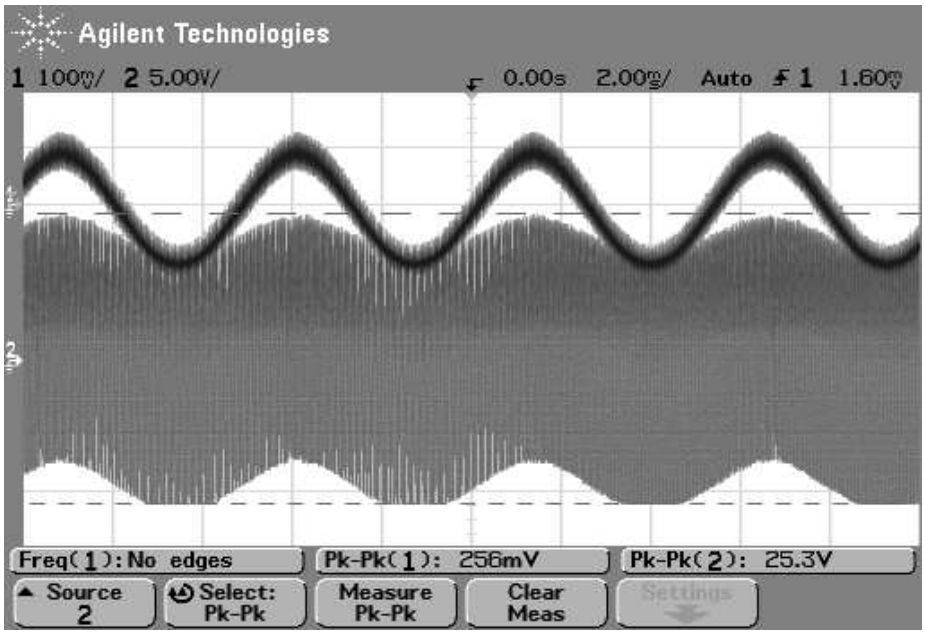

Figure 12: Low Gain Instability - Experiment 7

As we turned the potentiometer to produce higher gains, the noise and instability of the output signal decreased greatly. While we were not able to quite reach stability with a gain of approximately 100, if we manually adjusted the

resistors, and used a gain of higher than 100, we found stability. We have included another oscilloscope trace on page 15 demonstrating the near stability when the gain was 100.

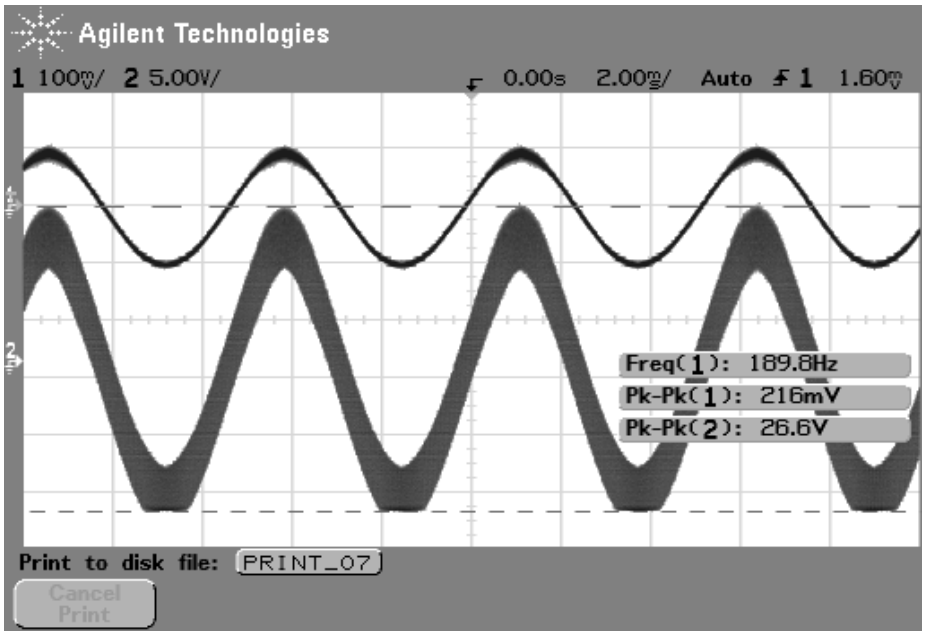

Figure 13: High Gain Near-Stability - Experiment 7

2.8 Dominant-Pole Compensation

To eliminate the instability of the previous circuit, we can employ a method called "Dominant-Pole Compensation", which can eliminate instability at the cost of reduced gain. We introduce a pole in the amplifier's frequency response at at very low frequency. As visible in the circuit schematic on page 16, we have added an RC-filter between stages 1 and 2. This has the effect of adding a pole at $f_{dp} = \frac{1}{2\pi R_{dp} C_{dp}}$.

To calculate the required frequency of the dominant pole, we can use an equation derived from the Bode Plot analysis.

$$20\log(A_{45^\circ} \cdot \beta) = 10\log\left[1 + \left(\frac{f_{45^\circ}}{f_{dp}}\right)^2\right]$$

Where A_{45° is the open-loop gain of the amplifier when the phase between the input and output signals is 45°. β is the feedback valuewe are designing for, which is 0.1 in this case. f_{45° is the frequency when the open-loop circuit has a

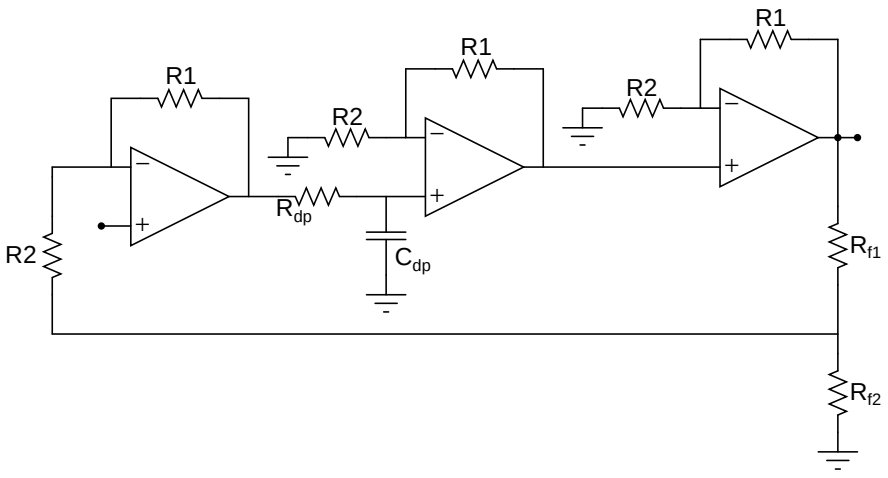

Figure 14: Circuit Schematic - Experiment 8

45° phase. f_{dp} is the frequency of the dominant pole compensation, and is the value we are searching for.

$$20\log(3250 \cdot 0.1) = 10\log\left[1 + \left(\frac{16.66K}{f_{dp}}\right)^2\right]$$

$$f_{dp} = 51.26Hz$$

We can now solve for the resistor and capacitor to use in the RC-circuit filter. We choose the largest capacitor we have access to, a 0.1 μF capacitor.

$$51.26 = \frac{1}{2\pi R(0.1\mu F)} \Rightarrow R = 32K\Omega$$

We can use a $10K\Omega$ resistor and a $22K\Omega$ resistor to create this required value.

After adding the dominant pole compensation, we immediately notice an improvement in stability across all frequencies. A sample of the stable operation is included on page 17. If we turn up our frequency generators until we reach the 0 dB frequency, where the input and output signals have the same magnitude, we can determine the phase margin of our compensated amplifier. We find that the phase is approximately 127°, which is well below the required phase of 180°. The phase margin is simply the difference between 180° and the measured phase. We have a phase margin of about 53°, well withing the specified range of 45° - 90°.

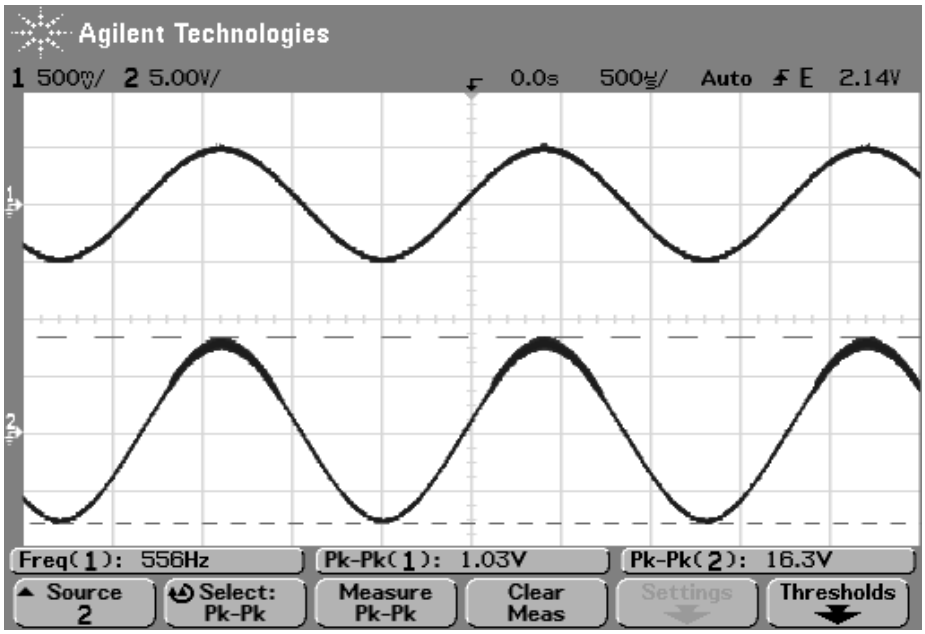

Figure 15: Example of Stability - Experiment 8

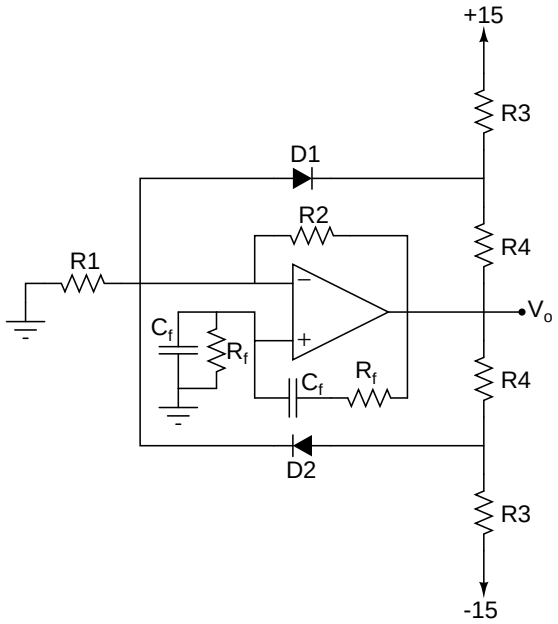

Figure 16: Circuit Schematic - Experiment 9

2.9 Sinusoidal Oscillator

As mentioned in the introduction, if we employ positive, frequency selective feedback with an amplitude limiting circuit, we can create a circuit that oscilates on its own, and creates sine wave output. The design we have selected is the Wein-bridge oscilator, which uses a pair of RC circuits to impliment the frequency-selective feedback loop. We use a series of resistors and diodes to impliment the amplitude limiter. The values of R_1 and R_2 determine the loop gain of the circuit, and the ratio of $\frac{R_2}{R_1}$ should be slightly greater than 2. This ensures that there will be sufficient gain for oscillation to occur.

Since we want our oscilator to operate at 500 Hz, we use the following relation to find the values of the feedback resistors and capacitors.

$$f = \frac{1}{2\pi RC}$$

We arbitrarily select the largest available capacitor, $0.1\mu F$. This choice specifies the resistor to be 3.2 k Ω.

We now need to set the values for R_3 and R_4. We start with selecting $R_4 = 1K\Omega$, and then try various values for R_3, until we observe an output signal with amplitude of 5v. We find that having $R_3 = 6.1K\Omega = 5.1K\Omega + 1.0K\Omega$ works nicely. We have included an example of the output waveform on page 17. You can clearly see that we have acheived all design goals, including an oscilation frequency of about 500 Hz, and peak-to-peak output voltage of about 10v.

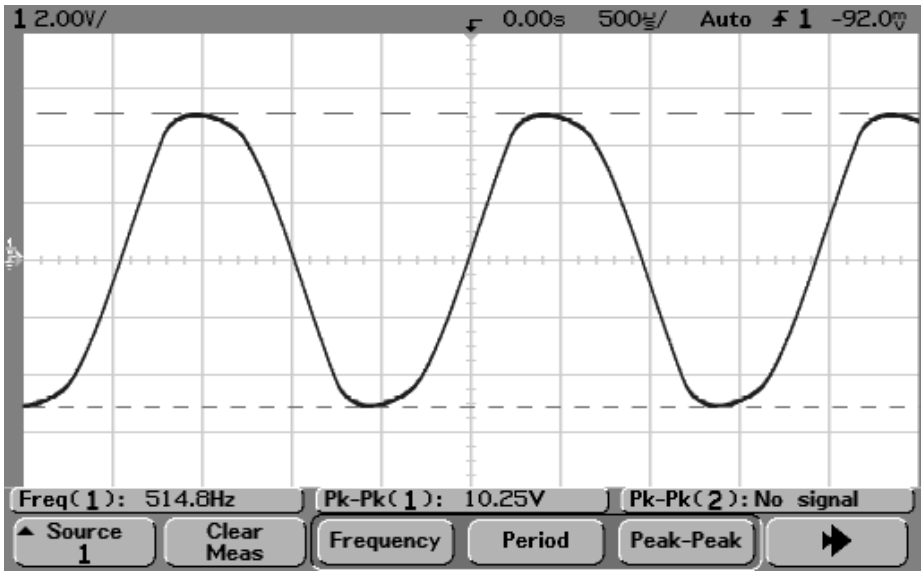

Figure 17: Oscilator Output - Experiment 9

3 Conclusion

Through the course of this experiment, we have investigated many aspects of feedback in amplifier design. We have explored all four negative feedback topologies, and how loading affects each topology. We also experimented with multi-stage amplifiers, both with a two-stage design, and a three-stage design. With the three-stage design, we noticed rampant instability caused by having a phase of 180°, which was subsequently corrected through the design and implimentation of a dominant-pole compensation element. If positive feedback is not compensated, oscillation can occur, and sometimes this is a desired trait. We can purposely design for oscillation, using a frequency-sensitive feedback network to select our desired frequency. We used such a circuit to create a sine wave generating circuit.